REMARKS/ARGUMENTS

Claims 1-44 were originally presented.

Claims 1 and 6-8 are currently amended.

No claims are canceled.

Claim 1 is objected to on the basis of a formality.

Claims 8, 15, 30 and 38 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

Claims 6-8 are objected to on the basis of insufficient antecedent basis.

Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39, and 40-44 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,799,168 to Ban (hereinafter "Ban").

Claims 2, 12, 20, 27 and 35 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of U.S. Patent No. 6,000,006 to Bruce *et al.* (hereinafter "Bruce").

Claims 3-4, 13-14, 19, 21, 26, 28, 34 and 36 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of U.S. Patent No. 6,493,807 to Martwick (hereinafter "Martwick").

Claims 1-44 remain in this application.

35 U.S.C. §112 first paragraph

Claims 8-9, 15-16, 21-24, and 28-31

Claims 8, 15, 30, and 38 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written restriction requirement. The Office asserts that the claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s) at the time the application was filed had possession of the claimed invention. In particular, the Office asserts that the specification fails to describe how the flash medium logic performs error code correction. (*Office Action*, Page 3). Applicant respectfully traverses the rejection.

The specification states "[e]ach sector 102 is further divided into two distinct sections, a data area 103 used to store information and a spare area 104 which is used to store extra information such as error correction code (ECC)." (Page 5, lines 17-19). In addition the specification also discloses:

> The flash medium logic 310 is also responsible for performing ECC (if necessary). In one implementation, the flash medium logic 310 is programmable to permit users to match particular flash medium requirements of a specific manufacturer. Thus, the flash medium logic 310 is configured to handle specific nuances, ECC, and specific commands associated with controlling physical aspects of flash medium 100/200.
>
> FIG. 5 illustrates an exemplary block diagram of the flash medium logic 310. As shown, the flash medium logic 310 includes a programmable entry point module 502, I/O module 504 and an ECC module 506. The programmable entry point module 502 defines a set of programming interfaces to communicate between flash abstraction logic 308 and flash medium 100/200. In other words, the programmable entry points permit manufacturers of computer devices 300 to program the flash media logic 310 to interface with the actual flash memory medium 100/200 used in the computer device 300. The I/O module 504 contains specific code necessary

> for read/write/erase commands that are sent to the Flash memory medium 100/200. The user can program the ECC module 506 to function in accordance with any particular ECC algorithm selected by the user. (Page 11 line 12 - Page 12 line 3).

Thus the subject matter contained in claims 8, 15, 30 and 38 is described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s) at the time the application was filed had possession of the claimed invention. Accordingly, the rejection of claims 8, 15, 30 and 38 under 35 U.S.C. §112, first paragraph, is improper. Applicant respectfully requests that the rejection be withdrawn

35 U.S.C. §102(b)

Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39, and 40-44

Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39, and 40-44 are rejected under 35 U.S.C. §102(b) as being anticipated by Ban. Applicant respectfully traverses the rejection.

As a preliminary note, Ban's entire Description of the Preferred Embodiments section is contained in column 5 and includes a mere 30 lines of text. As a result, in many instances it is completely unclear to one skilled in the art what is being taught in Ban. This notwithstanding, Applicant has done its best to understand Ban. Any further help from the Office towards this aim would be greatly appreciated.

Amended independent claim 1 recites:

> One or more computer-readable media comprising a flash memory driver that is executable by a computer to interface between a file system and one or more flash memory media, the flash memory driver comprising:
>
> flash abstraction logic that is invokable by the file system to manage flash memory operations without regard to the type of the one or more flash memory media; and
>
> flash media logic configured to interact with different types of the flash memory media;
>
> wherein the flash abstraction logic invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media.

Ban fails to disclose the one or more computer-readable media comprising a flash memory driver of claim 1. Rather, as best as Applicant understands Ban, Ban discloses shifting the responsibility for conforming to the particular requirements of a flash chip from a driver installed on a CPU to a controller installed on a flash unit. (Ban, Col. 2, lines 44-46). The CPU sends out commands necessary to perform flash memory tasks in a uniform, standardized format. (Ban Col. 2, lines 42-43). The standardized commands (read, write, erase and identify) are received via a command register and are translated by the standardized controller on the flash unit (through a translating apparatus) into commands specific to the type of flash chip on which the controller is installed. (Ban, Col. 3, lines 1-15 and Col. 5, lines 29-33). Thus, when a flash array including multiple flash chips is used, rather than having a single flash driver to communicate with all of the flash chips, as best as Applicant understands Ban, a controller must be placed on each flash chip. (Ban, Col. 4, lines 33-35, claim 2 lines 29-30).

In one such configuration, the controllers are connected in a daisy chain. (Ban, Col. 4, lines 52-53). When the first controller receives an identify command, it takes its identify information and passes it on to the next controller which

produces its own identify information and adds its size to the size received from the previous controller. (Ban Col. 4, lines 53-56). This proceeds until all the controllers in the array have been polled and the result returned by the last controller is returned to the CPU. (Ban, Col. 4, lines 57-60).

Thus, as best as Applicant understands Ban, a command sent from the CPU may potentially go through several standardized controllers before it is received in the standardized controller residing on the flash chip for which the command was intended. Moreover, the possible output from the CPU is limited to standardized signals. Thus multiple file systems having multiple signal types may not be used under Ban.

As a result, Ban fails to disclose "flash abstraction logic that is invokable by the file system to manage flash memory operations without regard to the type of the one or more flash memory media" as recited in claim 1. Rather, as best as Applicant understands Ban, the responsibility for conforming to the particular requirements of a flash chip is given to a controller installed on an individual flash chip. Thus the controllers used under Ban are flash chip specific, and cannot be used with other types of flash chips. Therefore, each time a new flash chip is used, a new controller that is compatible with the new flash chip must be located on the flash chip. Because of this, the controllers of Ban are also ill-equipped "to interact with different types of the flash memory media" as recited in claim 1.

Moreover, Ban fails to disclose "wherein the flash abstraction logic invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media". Rather, under Ban the controllers are bound to a particular flash chip and thus are limited to performing memory operations specific to that flash chip.

In rejecting claim 1, the Office relies on Fig.1, claim 2 and the Abstract (Col. 2, lines 36-48) of Ban. (*Office Action*, Pages 3-4). However, the elements of claim 1 are neither disclosed in the cited passages nor anywhere else within Ban. As noted above, multiple flash chips would require a like number of controllers located on each flash chip under Ban. This teaches against a single "flash abstraction logic that is invokable by the file system to manage flash memory operations without regard to the type of the one or more flash memory media".

Accordingly, since Ban does not teach all of the elements of claim 1, the §102(b) anticipation rejection of claim 1 based on Ban is not supported. Applicant therefore respectfully requests that the §102(b) rejection of claim 1 be withdrawn.

Dependent claims 5-7 are allowable at the least by virtue of their dependency on base claim 1, as well as for the additional elements they contain. For example, **amended dependant claim 6** recites:

> The flash memory driver as recited in Claim 1, wherein the flash medium logic is further configured to translate commands received from the file system to physical sector commands for issuance to the flash memory media.

In rejecting claim 6, the Office relies on Ban, Col. 5, lines 29-37. (*Office Action*, Page 4). However, the elements of claim 6 are neither disclosed in the cited passage nor anywhere else within Ban. Rather, as best as Applicant understands Ban, during a read write operation, the CPU specifies the flash address at which the read/write operation shall take place. (Ban, Col. 3, lines 43-45). Thus, Ban teaches away from the flash memory driver and flash medium logic disclosed in claim 6, by requiring the CPU -- rather than the flash driver -- to coordinate and organize all mappings between a computer's memory and a flash array.

Thus, in addition to Ban's failings stated above in conjunction with claim 1, Ban also fails to disclose "wherein the flash medium logic is further configured to translate commands received from the file system to physical sector commands for issuance to the flash memory media" as recited in claim 6.

Applicant respectfully requests that the §102(b) rejection of claims 5-7 be withdrawn.

Independent claim 9 recites:

A flash driver, comprising:

flash abstraction logic, interposed between a file system and a flash memory medium, configured to:

(a) map a logical sector status from the file system to a physical sector status of the flash memory medium; and

(b) maintain memory requirements associated with operating the flash memory medium.

Ban fails to disclose the flash driver of claim 9. In particular, under Ban during a read write operation the CPU specifies the flash address at which a read/write operation shall take place. (Ban, Col. 3, lines 43-45). Thus, the CPU, rather than the flash driver, must coordinate and organize all mappings between a computer's file system (using, for example, logical sector addressing) and the flash array (using, for example, physical sector addressing). This is the opposite of a "flash driver, comprising: flash abstraction logic, interposed between a file system and a flash memory medium, configured to: (a) map a logical sector status from the file system to a physical sector status of the flash memory medium; and (b) maintain memory requirements associated with operating the flash memory medium".

In rejecting claim 9, the Office relies on the same bases as used in the rejection of claim 1, namely Fig.1, claim 2 and the Abstract (Col. 2, lines 36-48) of Ban. (*Office Action*, Page 3). However, the elements of claim 9 are neither disclosed in the cited passages nor anywhere else within Ban. As discussed more fully above in conjunction with claim 1, in the passages relied on by the Office, the standardized commands received via a command register are read, write, erase and identify. However, the CPU, and not the flash driver, provides the flash address at which a read or write operation is to take place.

Accordingly, since Ban fails to show each and every element of claim 9 the §102(b) rejection of claim 9 based on Ban is not supported. Applicant therefore respectfully requests that the §102(b) rejection of claim 9 be withdrawn.

Dependent claims 10-11 are allowable due to their dependence from an allowable base claim. These claims are also allowable for their own recited features that, in combination with those recited in claim 9, are neither disclosed nor suggested in Ban. Applicant therefore respectfully requests that the §102(b) rejection of claims 10 and 11 be withdrawn.

Independent claim 16 recites:

A flash driver, comprising:

user programmable flash medium logic, configured to read, write and erase data to and from a flash memory medium; and

flash abstraction logic, interposed between a file system and flash memory medium to maintain universal requirements for the operation of the flash memory medium.

Ban fails to disclose the flash driver of claim 16. Rather, as discussed in more detail above, Ban teaches the use of flash chip specific controllers, such that for each flash chip used, a separate controller compatible with the flash chip must be employed on the flash chip. Thus, unlike claim 16, where programmable flash medium logic may be programmed by a user to interact with a flash memory medium, under Ban a new controller must be chosen to interact with each new flash chip.

In rejecting claim 16, the Office relies on the same bases as used in the rejection of claim 1 -- namely Fig.1, claim 2 and the Abstract (Col. 2, lines 36-48) of Ban --- in addition to claim 7, and Col. 3. lines 19-24 of Ban. (*Office Action*, Page 3). However, as noted above in conjunction with claim 1, these passages fail to disclose or show "user programmable flash medium logic, configured to read, write and erase data to and from a flash memory medium". Accordingly, Applicant respectfully requests that the §102(b) rejection of claim 16 be withdrawn.

Dependent claims 17 and 22 are allowable at the least by virtue of their dependency on base claim 16, as well as for the additional elements they contain. Applicant respectfully requests that the §102(b) rejection of claims 17 and 22 be withdrawn.

Independent claim 23 recites:

A processing device that uses a flash memory medium for storage of data, comprising:

a file system, configured to control data storage for the processing device;

flash media logic, configured to perform physical sector operations to a flash memory medium based on physical sector commands, wherein the flash medium logic comprises a set of programmable cntry points that can be implemented by a user to interface with the type of flash memory medium selected; and

flash abstraction logic, configured to maintain flash memory requirements that are necessary to operate the flash memory medium.

Ban fails to disclose the processing device of claim 23. As noted above, under Ban a separate compatible controller must also be used for each flash chip employed. This is different than a flash media logic including "a set of programmable entry points that can be implemented by a user to interface with the type of flash memory medium selected" disclosed in claim 23. The difference lies in the fact that the flash media logic of claim 23 may easily be used with multiple, different flash chips. In contrast, under Ban, multiple controllers would be needed to interface with multiple flash chips.

In rejecting claim 23, the Office relies on Ban, Col. 2, lines 17-23; Col. 3, lines 15-24; Col. 2, lines 36-48 and Fig 1. (*Office Action*, Page 5). Applicant respectfully disagrees. As noted above, Ban discloses using different controllers for different flash chips. Moreover, under Ban each controller is located on a flash chip. Thus, a flash medium logic compatible with several types of flash memory media makes no sense under Ban. Accordingly, Applicant respectfully requests that the §102(b) rejection of claim 23 be withdrawn.

Dependent claims 24-25, 29 and 31-32 are allowable at the least by virtue of their dependency on base claim 23, as well as for the additional elements they contain. Applicant respectfully requests that the §102(b) rejection of claims 24-25, 29 and 31-32 be withdrawn.

Independent claim 33 recites:

In a processing device that uses a flash memory medium for storage of data, a method for driving the flash memory medium, comprising:

managing rules associated with operating the flash memory medium in a flash abstraction logic; and

issuing physical sector commands directly to the flash memory medium from a flash medium logic.

Ban fails to disclose the processing device of claim 33. In particular, under Ban during a read write operation the CPU specifies the flash address at which a read/write operation shall take place. (Ban, Col. 3, lines 43-45). Thus, the CPU, rather than the flash driver, must coordinate and organize all mappings between a computer's file system (using, for example, logical sector addressing) and the flash array (using, for example, physical sector addressing). Therefore Ban does not disclose "issuing physical sector commands directly to the flash memory medium from a flash medium logic".

The Office argues that the claimed method for driving the flash memory medium is shown in Fig.1, claim 2, the Abstract (Col. 2, lines 36-48), claim 7, and Col. 3. lines 19-24 of Ban. (*Office Action*, Page 3). Applicant respectfully disagrees. As noted above, under Ban the CPU, and not the flash driver, provides the flash address at which a read or write operation is to take place. Thus, as best as Applicant understands Ban, the CPU, rather than the flash driver, must coordinate and organize all mappings between a computer's file system (using, for example, logical sector addressing) and the flash array (using, for example, physical sector addressing). Accordingly, Applicant respectfully requests that the §102(b) rejection of claim 33 be withdrawn.

Dependent claims 37 and 39-41 are allowable at the least by virtue of their dependency on base claim 33, as well as for the additional elements they contain. Applicant respectfully requests that the §102(b) rejection of claims 37 and 39-41 be withdrawn.

Independent claim 42 recites:

A computer-readable medium for a flash driver, comprising computer-executable instructions that, when executed, direct the flash driver to provide an interface between a file system, selected from one of a plurality of different file systems, and a flash memory medium, selected from one of a plurality of different flash memory media.

Ban fails to disclose the computer readable medium for a flash driver of claim 42. As discussed above, under Ban the responsibility for conforming to the particular requirements of a flash chip is given to a controller installed on an individual flash chip. Thus the controllers used under Ban are flash chip specific, and are limited to providing an interface for only one specific chip. Therefore, a single controller under Ban cannot provide an interface between "one of a plurality of different flash memory media" as disclosed in claim 42. Rather, under Ban, in order to provide an interface with more than one different flash chip, an equivalent number of controllers would be needed, with one controller being located on each flash chip. Therefore, Ban does not disclose "comprising computer-executable instructions that, when executed, direct the flash driver to provide an interface between a file system, selected from one of a plurality of different file systems, and a flash memory medium, selected from one of a plurality of different flash memory media".

The Office argues that the claimed computer-readable medium is shown in Fig.1, claim 2 and the Abstract (Col. 2, lines 36-48) of Ban. (*Office Action*, Page 6). Applicant respectfully disagrees. These passages disclose placing separate controllers on each flash chip in an array in order to interface with a CPU. Thus no one controller can interface with a flash memory medium, selected from one of a plurality of different flash memory media. Accordingly, Applicant respectfully requests that the §102(b) rejection of claim 42 be withdrawn.

Independent claim 43 recites:

A computer-readable medium for a flash driver, comprising computer-executable instructions that, when executed, direct the flash driver to:

provide an interface between a file system, selected from one of a plurality of different files systems, and a flash memory medium, selected from one of a plurality of different flash memory media; and

manage a set of characteristics that are common to the plurality of different flash memory media at a flash abstraction logic.

Ban fails to disclose the computer-readable medium for a flash driver of claim 43. Similar to claim 42 above, under Ban, the responsibility for conforming to the particular requirements of a flash chip is given to a controller installed on the flash chip itself. Thus the controllers used under Ban are flash chip specific, and can provide an interface for only one chip. Therefore, a single controller under Ban cannot provide an interface between "one of a plurality of different flash memory media" as disclosed in claim 43. Rather, under Ban, in order to provide an interface with more than one different flash chip, an equivalent number of controllers would be needed, with one controller being located on each flash chip. Therefore Ban does not disclose "provide an interface between a file system,

selected from one of a plurality of different files systems, and a flash memory medium, selected from one of a plurality of different flash memory media".

Moreover, since the controllers disclosed in Ban are flash chip specific, it would take a plurality of controllers to manage characteristics common to a plurality of flash chips. Therefore, Ban does not teach "manage a set of characteristics that are common to the plurality of different flash memory media at a flash abstraction logic". Rather, under Ban a plurality of controllers having flash abstraction logic would be required to fulfill this function.

The Office argues that the same passages cited with regard to claim 42 above disclose the claimed computer-readable medium claimed in claim 43. (*Office Action*, Page 6). Applicant respectfully disagrees. As noted above, these passages disclose placing separate controllers on each flash chip in an array in order to interface with a CPU. Thus, under Ban no one controller can interface with a flash memory medium, selected from one of a plurality of different flash memory media, and no one controller can manage a set of characteristics common to a plurality of different flash memory media at a flash abstraction logic. Accordingly, Applicant respectfully requests that the §102(b) rejection of claim 43 be withdrawn.

Independent claim 44 recites:

A computer-readable medium for a flash driver, comprising computer-executable instructions that, when executed, direct the flash driver to:

provide an interface between a file system, selected from one of a plurality of different files systems, and a flash memory medium, selected from one of a plurality of different flash memory media;

manage a set of characteristics that are common to the plurality of different flash memory media at a flash abstraction logic; and

provide programmable entry points that can be optionally selected by a user to interface with the type of flash memory medium selected.

Ban fails to disclose the computer-readable medium for a flash driver of claim 44. As discussed above, under Ban the responsibility for interfacing with the particular requirements of a flash chip is given to a controller installed on an individual flash chip. Thus the controllers used under Ban are flash chip specific, and can provide an interface for only one chip. Therefore, a single controller under Ban cannot provide an interface between "a file system, selected from one of a plurality of different files systems, and a flash memory medium, selected from one of a plurality of different flash memory media". Moreover, it also follows that a controller under Ban cannot "manage a set of characteristics that are common to the plurality of different flash memory media at a flash abstraction logic". To achieve this sort of functionality, Ban would require a plurality of controllers rather that the single flash driver recited in claim 44.

In addition, since a controller under Ban is configured to interface with a particular flash chip -- and is even located on a particular flash chip -- a controller could not be used to "provide programmable entry points that can be optionally selected by a user to interface with the type of flash memory medium selected". This would imply that a controller disclosed in Ban could work with several different flash chips, which it can't. Moreover, there is no disclosure in Ban which mentions "programmable entry points that can be optionally selected by a user". Rather, under Ban the user's choice consists solely of which controller to use with a given flash chip.

The Office argues that the claimed computer-readable medium is shown in same passages used to reject claim 7 above, namely Ban, Col. 3, lines 19-24.

(*Office Action*, Page 6). Applicant respectfully disagrees. Ban discloses only controllers that are configured for a one type of flash chip. Thus the versatility recited in claim 44 above would be impossible under Ban. Accordingly, Applicant respectfully requests that the §102(b) rejection of claim 44 be withdrawn.

35 U.S.C. §103(a)

The remaining claims are rejected under a set of §103 rejections, all of which rely on Ban as the primary reference. Moreover, all of these claims depend from base claims addressed above.

Ban +Bruce

Claims 2, 12, 20, 27 and 35 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of Bruce. Applicant respectfully traverses the rejection.

Claims 2, 12, 20, 27 and 35 depend from respective independent claims 1, 9, 16, 23, and 33. As such, they include the features recited in those base claims. The combination of Ban and Bruce fails to teach or suggest the features of these base claims from which the cited claims depend. Ban is primarily cited as teaching the base features, and Bruce is cited as teaching the use of a unified remapping and wear leveling table to overcome the disadvantages of the larger granularity of block remapping.

With respect to **dependent claim 2**, neither reference discloses, "flash abstraction logic that is invokable by the file system to manage flash memory operations without regard to the type of the one or more flash memory media" as recited in claim 1 from which claim 2 depends. Ban specifically teaches giving the

responsibility for conforming to the particular requirements of a flash chip to a controller installed on an individual flash chip. Thus the controllers used under Ban are flash chip specific, and cannot be used with other types of flash chips. Therefore, each time a new flash chip is used, a new controller that is compatible with the new flash chip must be located on the flash chip.

In addition, neither reference discloses, teaches or suggests "flash media logic configured to interact with different types of the flash memory media" or "wherein the flash abstraction logic invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media". Instead, Ban teaches that the controllers are bound to a particular flash chip and thus are limited to performing memory operations specific to that flash chip. Thus interacting with different types of flash memory media would require several controllers rather that the single flash memory driver recited in claim 1 from which claim 2 depends.

Bruce offers no missing teaching. Accordingly, the combination of Ban and Bruce fails to teach or suggest the device of claim 2. Applicant respectfully requests that the §103 rejection of claim 2 be withdrawn.

With respect to **dependant claim 12,** neither reference discloses "flash abstraction logic, interposed between a file system and a flash memory medium, configured to: (a) map a logical sector status from the file system to a physical sector status of the flash memory medium" as recited by claim 9 from which claim 12 depends. Rather Ban teaches away from this by disclosing that during a read write operation the CPU specifies the flash address at which a read/write operation shall take place. Thus, under Ban the CPU, rather than the flash driver, coordinates and organizes all mappings between a computer's file system (using,

for example, logical sector addressing) and the flash array (using, for example, physical sector addressing).

Again, Bruce offers no missing teaching. Accordingly, the combination of Ban and Bruce fails to teach or suggest the device of claim 12. Applicant respectfully requests that the §103 rejection of claim 12 be withdrawn.

With respect to **dependant claim 20**, for the reasons just given, neither reference teaches or suggests "user programmable flash medium logic, configured to read, write and erase data to and from a flash memory medium". Accordingly, the combination of Ban and Bruce fails to teach or suggest the device of claim 20. Applicant respectfully requests that the §103 rejection of claim 20 be withdrawn.

With respect to **dependant claim 27,** neither reference teaches or suggests "a set of programmable entry points that can be implemented by a user to interface with the type of flash memory medium selected" disclosed in claim 23 from which claim 27 depends. Ban teaches that a separate compatible controller must be used for each flash chip employed. This teaches away from the processing device of claim 27 which may be used with multiple, different flash chips. In contrast, under Ban, multiple controllers would be needed to interface with multiple flash chips.

Again, Bruce offers no relevant teaching. Applicant respectfully requests that the §103 rejection of claim 27 be withdrawn.

With respect to **dependant claim 35,** neither reference discloses, teaches or suggests "issuing physical sector commands directly to the flash memory medium from a flash medium logic" as recited in claim 33 from which claim 35 depends. Ban teaches that during a read write operation the CPU specifies the flash address at which a read/write operation shall take place. Thus, Ban teaches away from claim 33 and claim 35, which depends from claim 33, by specifying that the CPU,

rather than the flash driver, must coordinate and organize all mappings between a computer's file system (using, for example, logical sector addressing) and the flash array (using, for example, physical sector addressing).

Again, Bruce offers no relevant teaching. Applicant respectfully requests that the §103 rejection of claim 35 be withdrawn.

Ban + Martwick

Claims 3-4, 13-14, 19, 21, 26, 28, 34, and 36 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of Martwick. Applicant respectfully traverses the rejection.

Claims 3-4, 13-14, 19, 21, 26, 28, 34, and 36 depend from respective independent claims 1, 9, 16, 23, and 33. As such, they include the features recited in those base claims. The combination of Ban and Bruce fails to teach or suggest the features of the base claims from which the cited claims depend. Ban is primarily cited as teaching the base features, and Martwick is cited as teaching a method for updating flash blocks so that data integrity gets maintained and data can be recovered upon a power failure.

Dependent claims 3 and 4 depend from claim 1, and hence include the features therein. Neither reference discloses, "flash abstraction logic that is invokable by the file system to manage flash memory operations without regard to the type of the one or more flash memory media" as recited in claim 1. As noted above, Ban specifically teaches giving the responsibility for conforming to the particular requirements of a flash chip to a controller installed on an individual flash chip. Thus the controllers used under Ban are flash chip specific, and cannot be used with other types of flash chips. Therefore, each time a new flash chip is

used, a new controller that is compatible with the new flash chip must be located on the flash chip.

In addition, neither reference discloses, teaches or suggests "flash media logic configured to interact with different types of the flash memory media" or "wherein the flash abstraction logic invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media". Ban teaches that the controllers are bound to a particular flash chip and thus are limited to performing memory operations specific to that flash chip. Thus interacting with different types of flash memory media would require several controllers rather that the single flash memory driver recited in claim 1 from which claims 3 and 4 depend.

Martwick fails to add any relevant teaching with respect to these features. Accordingly, the combination of Ban and Martwick fails to teach or suggest the device of claims 3 and 4. Applicant respectfully requests that the §103 rejection of claims 3 and 4 be withdrawn.

Similarly **dependant claims 13 and 14** depend from base claim 9 and thus include the features therein.

Ban fails to teach or suggest "flash abstraction logic, interposed between a file system and a flash memory medium, configured to: (a) map a logical sector status from the file system to a physical sector status of the flash memory medium" as recited by claim 9. As previously discussed, Ban teaches away from this by disclosing that during a read write operation the CPU specifies the flash address at which a read/write operation shall take place. Thus, under Ban the CPU, rather than the flash driver, coordinates and organizes all mappings between a computer's

file system (using, for example, logical sector addressing) and the flash array (using, for example, physical sector addressing).

Again, Martwick offers no missing teaching. Accordingly, the combination of Ban and Martwick fails to teach or suggest the device of claims 13 and 14. Applicant respectfully requests that the §103 rejection of claims 13 and 14 be withdrawn.

Dependant claims 19 and 21 depend from base claim 16 and hence include the features therein. For the reasons just given, neither reference teaches or suggests "user programmable flash medium logic, configured to read, write and erase data to and from a flash memory medium". Accordingly, the combination of Ban and Martwick fails to teach or suggest the devices of claims 19 and 21. Applicant respectfully requests that the §103 rejection of claims 19 and 21 be withdrawn.

Dependant claims 26 and 28 depends from base claim 23 and hence include the features therein. Neither reference teaches or suggests "a set of programmable entry points that can be implemented by a user to interface with the type of flash memory medium selected" disclosed in claim 23 from which claims 26 and 28 depend. Ban teaches that a separate compatible controller must be used for each flash chip employed. This teaches away from the processing device of claims 26 and 28, which may be used with multiple, different flash chips. In contrast, under Ban multiple controllers would be needed to interface with multiple flash chips.

Again, Martwick offers no relevant teaching. Applicant respectfully requests that the §103 rejection of claims 26 and 28 be withdrawn.

Similarly, **dependant claims 34 and 36** depend from base claim 33 and hence include the features therein. Neither reference discloses, teaches or suggests "issuing physical sector commands directly to the flash memory medium from a flash medium logic" as recited in claim 33 from which claims 33 and 36 depend. Ban teaches that during a read write operation the CPU specifies the flash address at which a read/write operation shall take place. Thus, Ban teaches away from claims 33, 34 and 36 by specifying that the CPU, rather than the flash driver, must coordinate and organize all mappings between a computer's file system (using, for example, logical sector addressing) and the flash array (using, for example, physical sector addressing).

Again, Martwick offers no relevant teaching. Applicant respectfully requests that the §103 rejection of claims 34 and 36 be withdrawn.

CONCLUSION

All pending claims 1-44 are in condition for allowance. Applicant respectfully requests reconsideration and prompt issuance of the subject application. If any issues remain that prevent issuance of this application, the Examiner is urged to contact the undersigned attorney before issuing a subsequent Action.

Respectfully Submitted,

Dated: July 26, 2005

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